Ref No:

SRI KRISHNA INSTITUTE OF TECHNOLOGY, BANGALORE

COURSE PLAN

Academic Year 2019-20

Program:	B E – Electronics and Communication Engineering
Semester :	3
Course Code:	18EC34
Course Title:	Digital System Design
Credit / L-T-P:	3 / 4-0-0
Total Contact Hours:	40
Course Plan Author:	Kiranmayi M

Academic Evaluation and Monitoring Cell

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Note : Remove "Table of Content" before including in CP Book

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	EC
Semester:	3	Academic Year:	2019–20
Course Title:	Digital System Design	Course Code:	18EC34
Credit / L–T–P:	4 / 4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	40 Hours	SEE Marks:	60 Marks
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	Kiranmayi M	Sign ..	Dt:
Checked By:		Sign ..	Dt:
CO Targets	CIA Target : ……. %	SEE Target:	……. %

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute. Identify 2 concepts per module as in G.

Module	Content	Teaching Hours	Identified Module Concepts	Blooms Learning Levels
1	Definition of combinational, canonical forms, Generation of switching equations from truth tables, Karnaugh maps–3, 4 and 5 variables. Incompletely specified functions (Don't care terms). Simplifying max – term equations. Quine –McClusky minimization technique, Quine – McClusky using don't care terms, Reduced Prime Implicant tables.	8	Boolean function simplification	L2, L3

2	General approach, Decoders-BCD decoders, Encoders. Digital multiplexers-using multiplexers as Boolean function generators. Adders and Subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.	8	Combinational & Arithmetic circuits design	L4
3	Basic Bistable element, Latches, SR latch, application of SR latch, A Switch debouncer, The gated SR latch. The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops, The master-slave JK Flip-Flop. Characteristic equations, Registers, Counters-Binary Ripple Counter, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 counters using clocked JK Flip-Flops Design of a Synchronous Mod-6 counter using clocked D, T, or SR Flip Flops	8	Sequential Circuits design	L4
4	Introduction, Mealy and Moore models, State machine notation, synchronous sequential circuit analysis and design. Construction of state Diagrams, Counters Design.	8	State machines & Sequential circuit design	L2, L4
5	**Module 5: Applications of Digital Circuits,** Design of a Sequence Detector, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Guidelines for construction of state graphs, Design of Sequential Circuits using CPLDs, Design of Sequential Circuits using ROMs, Design of Sequential Circuits usingPLAs,and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider.	8	Sequential Ciruit design using PLA's and PLD's	L3
-		40	-	-

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes

2. Design: Simulation and design tools used – software tools used ; Free / open source

3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Modules	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1,2,3, 4,5	Digital logic applications and design by John M Yarbrough	3,4,5,6, 7	In Lib / In Dept

1,2,3, 4,5	Logic Design by Sudhakar Samuel		1,2,3,4, 5,6,7,8	In Lib / In Dept
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**		**-**	**-**
1,2,3, 4,5	DSD by A P Godse			In Lib
C	**Concept Videos or Simulation for Understanding**		**-**	**-**
C1	Introduction to DSD: you tube: nptelhrd			
C2	Digital circuit simulation: YouTube: techtrainingonline			
C3	Understanding basics of Flip Flops: Tecnitude GATE			
C4	Digital Logic Design:YouTube:scikidus			
C5	Digital Electronics Lectures:YouTube:Flyhigh Tutorials.			
D	**Software Tools for Design**			
	MultiSim Simulation tool, Pspice tool			
E	**Recent Developments for Research**		**-**	**-**
	Future trends in software engineering for mobile apps – https://ieeexplore.ieee.org/document/7476770			
F	**Others (Web, Video, Simulation, Notes etc.)**		**-**	**-**
1				
2				

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
5	18ELN15 /25	Basic Electronics	Digital Electronics	1/2		L2,L3

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.

Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level
1	FPGA development EdgeSparatan 6	Chip designing	Certificate courses for Electronics core industries placement	L4

| 2 | VeriLog | Simulation Tool | Hardware description language for logical syntesis | L4 |
| 3 | VHDL(VHSIC- HDL) | Electronic design automation | HDL for high speed integrated circuit | L4 |

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs. Identify a max of 2 Concepts per Module. Write 1 CO per Concept.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	18EC34.1	Understand the SOP & POS expressions & their simplifications from truth table.	4	Combinational circuits	Lecture	Assignment Unit Test & IA	L2 Understanding
1	18EC34.2	Solving max terms of SOP & POS using simplification techniques like k-map, Quine –McClusky minimization & Reduced Prime Implicant tables.	4	Boolean algebra	Lecture	Assignment Unit Test & IA	L3 Apply
2	18EC34.3	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	4	Boolean function generators	Lecture	Assignment Unit Test & IA	L4 Analyze
2	18EC34.4	Analyze & Design of Adders & Subs tractors using K-map	4	Ar–thematic circuits	Lecture	Assignment Unit Test & IA	L4 Analyze
3	18EC34.5	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.	4	Flip flops	Lecture	Assignment Unit Test & IA	L2 Understanding
3	18EC34.6	Analyze & Design of counters using clocked D,T or SR flip flops.	4	Counters	Lecture	Assignment Unit Test & IA	L4 Analyze

4	18EC34.7	Understand the Mealy & Moore models using their Block diagrams.	4	State machines	Lecture	Assignme nt Unit Test & IA	L2 Understand ing
4	18EC34.8	Analyze & Design of Sequential circuits using State & state transition technique.	4	Sequential circuit design	Lecture	Assignme nt Unit Test & IA	L4 Analyze
5	18EC34.9	Analyze and design sequential circuits using programmable logic devices	4	HDL	Lecture & PPT	Assignme nt Unit Test & IA	L4 Analyze
5	18EC34.10	Analyze and design applications of digital circuits	4	data-flow descriptio n	Lecture & PPT	Assignme nt Unit Test & IA	L4 Analyze
-	-	**Total**	**40**	-	-	-	**L2-L4**

2. Course Applications

Write 1 or 2 applications per CO.

Students should be able to employ / apply the course learnings to . . .

Mod ules	Application Area Compiled from Module Applications.	CO	Level
1	Used in design of adders, multiplexers, demultiplexers, decoders, encoders , comparators.	CO1	L2
2	Automated Cafeteria, home automation office automation etc	CO2	L3
2	To effective data exchange In communication system and to implement home alarm system, all digital devices including mobiles, laptops palmtops, notebooks etc	CO3	L4
4	In forming ALU for desinging CPU to GPU	CO4	L4
5	In formation of Registers, memory elements, counter design for digital clocks.	CO5	L2
6	To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO6	L4
7	To designing the sequential circuits & Can be used in video controller	CO7	L2
8	To design Elevator, vending machine, etc.	CO8	L4
9	Modern CPU's, computers, cell phones, digital clocks have finite state machine to control it	CO9	L4
10	Digital circuits found in high -tech devices like ALU, computer memory ,registers and microprocessors.	CO10	L4

3. Mapping And Justification

CO – PO Mapping with mapping Level along with justification for each CO-PO pair.

To attain competency required (as defined in POs) in a specified area and the knowledge & ability required to accomplish it.

Modules	Mapping		Mapping Level	Justification for each CO-PO pair	Level
-	CO	PO	-	'Area': 'Competency' and 'Knowledge' for specified 'Accomplishment'	-
	CO1	PO1	3	Applying the knowledge to simplify complex circuits.	L2
	CO2	PO1	3	Knowledge of Boolean algebra helps the students in circuit designing	L3
	CO2	PO2	3	Analysis of circuit provide the students for better understanding of digital circuits	L4
	CO3	PO1	3	Its sound foundation to analyze digital circuits	L4
	CO3	PO2	2	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
	CO3	PO3	2	Designing of complex combinational circuits	L4
	CO4	PO1	3	This knowledge required to design mathematical circuits	L2
	CO4	PO3	2	Designing of complex combinational circuits	L4
	CO4	PO4	2	Choose a simplified circuit for implementing a combinational circuit using an appropriate simplification method	L2
	CO5	PO2	2	Having knowledge in Flip flop and latches students could develop sequential circuit	L2
	CO5	PO3	2	Knowledge of Flip flops could be used to reduce the complexity of the sequential circuit	L2
	CO5	PO4	2	Having the knowledge in various sequential circuit design principles students could analyze the problem and come to a conclusion on which design principle to be use	L3
	CO6	PO1	3	Knowledge in counter design helps to find solutions for complex engineering problems in digital electronics	L4
	CO6	PO3	3	Knowledge in counter design helps digital electronics engineers to develop solutions for complex Engineering problems	L4
	CO6	PO4	2	Choose a simplified circuit for implementing a Sequential circuit using an appropriate Flip flop.	L2
	CO7	PO1	2	An understanding state models helps to design automated machines.	L4
	CO8	PO1	2	Knowledge in State Machines helps to find solutions for complex automated machines.	L2
	CO8	PO2	2	Knowledge in State Machines helps to analyze complex automated machines	L4
	CO8	PO3	2	Basic principles of State Machines help to design a complex automated machine.	L3
	CO9	PO1	2	Knowledge of programmable logic devices will help designing flexible digital circuits.	L3
	CO9	PO3	2	Fast and new digital circiuts can be designed with PLD's	L3

	CO10	PO1	2	Apply the suitable algorithms to design digital logic circuits	L3
	CO10	PO3	2	Knowledge required to know the flow of data graphically	L4

4. Articulation Matrix

CO – PO Mapping with mapping level for each CO–PO pair, with course average attainment.

–	–	Course Outcomes	Program Outcomes															–
Mod ules	CO.#	At the end of the course student should be able to . . .	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3	Lev el
1	18EC34.1	Understand the SOP & POS expressions & their simplifications from truth table.	X															L2
1	18EC34.2	Solving max terms of SOP & POS using simplification techniques like k-map, Quine –McClusky minimization & Reduced Prime Implicant tables.	X	X														L3
2	18EC34.3	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	X	X	X													L4
2	18EC34.4	Analyze & Design of Adders & Subs tractors using K-map	X		X	X												L4
3	18EC34.5	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.		X	X	X												L2
3	18EC34.6	Analyze & Design of counters using clocked D,T or SR flip flops.	X		X	X												L4
4	18EC34.7	Understand the Mealy & Moore models using their Block diagrams.	X															L2
4	18EC34.8	Analyze & Design of Sequential circuits using State & state transition technique.	X	X	X													L4
5	18EC34.9	Understand the structure of HDL, operators using block diagram & compare between VHDL & Verilog.	X		X													L2
5	18EC34.1 0	Understand the structure of Data flow description using	X		X													L2

		block diagram & flowchart.														
-	**CS501PC**	**Average attainment (1, 2, or 3)**														-
–	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning;*														

5. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping

6. Content Beyond Syllabus

Topics & contents required (from A.5) not addressed, but help students for Placement, GATE, Higher Education, Entrepreneurship, etc.

Modules	Gap Topic	Area	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1						
2						
3						
4						
5						

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation. Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Principles of combinational logic	10	2	–	–	1	1	2	CO1, CO2	4
2	Principles of combinational logic	12	2	–	–	1	1	2	CO3, CO4	4
3	Sequential Circuits	10	–	2	–	1	1	2	CO5,	4

								CO6	
4	Melay and Moore State machine Design	10	–	2	–	1	1	2	CO7, CO8	4
5	Applications of digital circuits	10	–	–	4	1	1	2	CO9, CO10	2
-	**Total**	**52**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1, CO2, CO3, CO4	L2, L3, L4, L4
3, 4	CIA Exam – 2	30	CO5, CO6, CO7, C08	L2, L4, L2, L4
5	CIA Exam – 3	30	CO9, CO10	L2, L2
1, 2	Assignment – 1	10	CO1, CO2, CO3, CO4	L2, L3, L4, L4
3, 4	Assignment – 2	10	CO5, CO6, CO7, CO8	L2, L4, L2, L4
5	Assignment – 3	10	CO9, CO10	L2, L2
1, 2	Seminar – 1		–	–
3, 4	Seminar – 2		–	–
5	Seminar – 3		–	–
1, 2	Quiz – 1		–	–
3, 4	Quiz – 2		–	–
5	Quiz – 3		–	–
1 – 5	Other Activities – Mini Project	–	–	–
	Final CIA Marks	**40**	**-**	**-**

D1. TEACHING PLAN – 1

Module – 1

Title:	Introduction to software process		Appr Time:	10Hrs
a	*Course Outcomes*		–	**Blooms**
–	The student should be able to:		–	**Level**
1	Understand the SOP & POS expressions & their simplifications from truth table.	CO1		L2
2	Solving max terms of SOP & POS using simplification techniques like k–	CO2		L3

	map, Quine –McClusky minimization & Reduced Prime Implicant tables.		

b	*Course Schedule*	–	–
Class No	**Module Content Covered**	**CO**	**Level**
1	Definition of combinational	C01	L2
2	canonical forms	CO1	L2
3	Generation of switching equations from truth tables,	CO1	L3
4	Karnaugh maps–3, 4 and 5 variables.	CO2	L3
5	Incompletely specified functions (Don't care terms).	CO2	L3
6	Simplifying max – term equations.	CO2	L3
7	Quine –McClusky minimization technique,	CO2	L3
8	Quine – McClusky using don't care terms,	CO2	L3
9	Reduced Prime Implicant tables.	CO2	L3
10	Reduced Prime Implicant tables.	CO2	L3

c	**Application Areas**	**CO**	**Level**
1	To express the boolean expressions	CO1	L2
2	To simplify the Switching equations	CO2	L3

d	**Review Questions**	–	–
1	Explain combinational logic Circuit with the help of block diagram	C01	L2
2	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP	C01	L2
3	What are the different ways of simplifying a Boolean expression	C01	L2
4	What are canonical forms illustrate with an example	C01	L2
5	Reduce the following function using K-Map technique and implement using Basic gates. a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	C01	L3
6	Reduce the following function using K-Map technique and implement using only the NAND gates. a. $f(A,B,C,D) = \sum(0,2,5,7,8,10,13,15) + dc(9,11)$ b. $f(A,B,C,D) = \prod(3,4,6,11,12,14), dc(7,15)$ c. $f(A,B,C,D) = \sum(1,3,4,6,9,11) + dc(5,7)$ d. $f(A,B,C,D) = \prod(0,1,2,5,9,11), dc(7,13)$	C01	L3
7	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$	C01	L3
8	Express the following SOP expressions into minterm list form and hence write maxterm list	C01	L3

	a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$		
9	Design a logic circuit with inputs P, Q, R so that output S is high whenever P is zero or whenever Q=R=1	C01	L3
10	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high, Use K – Map to simplify	C01	L3
11	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high, Use K – Map to simplify	C01	L3
12	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates	C01	L3
13	Staircase light is controlled by two switches; one is at the top of the stair and other at the bottom of the stairs. a.Make a truth table for this system. b.Write the logic equations in the SOP form. c.Realize the circuit using basic gates. Realize the circuit using minimum number of NAND gates	C01	L3
14	Design a combinational logic circuit, which converts BCD code into Excess-3 code and draw the circuit diagram.	C01	L3
15	Distinguish between prime implicants and essential prime implicants. Determine the same of the function using K-map & hence the minimal sum expression. $f(w,x,y,z) = \sum m(0,1,4,5,9,11,13,15)$	C01	L3
16	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	C01	L3
17	Express the Product of Sums equations in a maxterms list (decimal notations) form a. $f(a,b,c) = (a+b'+c)(a+b'+c)(a'+b'+c')$ b. $f(a,b,c,d) = (a+b'+c+d)(a+b'+c+d')(a'+b+c+d)(a'+b'+c+d)(a'+b+c'+d)(a'+b'+c'+d)$	C01	L3
18	Convert the Product of Sums expression to its Canonical form a. $f(a,b,c) = (a+b)(b+c)(a+c)$ b. $f(a,b,c) = a.(a+b+c)$ c. $f(a,b,c) = (b+c').(ab'+c)$	C01	L3
19	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$	C01	L3
20	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	C01	L3
21	Simplify using Quine McClusky tabulation algorithm $Y = f(a,b,c,d) = \sum m(2,3,4,5,13,15) + dc(8,9,10,11)$	CO2	L3
22	Simplify the logic function given below, using Quine - McClusky minimization technique. $Y(A,B,C,D) = \sum m(0,1,3,7,8,11,15)$. Realize the simplified expression using universal gates.	CO2	L3
23	Using Quine McClusky method and prime implicant reduction table,	CO2	L3

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	Obtain the Minimal sum expression for the function		
24	Obtain the minimal product of the following Boolean functions using (VEM) technique. $Y = f(a,b,c,d) = \sum m(1,5,7,10,11) + dc(2,3,6,13)$	CO2	L3
25	Simplify the following expression using Quine-McClusky technique and implement using basic gates. $f(A,B,C,D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	CO2	L3
26	Minimize $f(a,b,c,d) = \pi M(0,6,7,8,9,13) + \pi d(5,15)$ using Quine – McClusky method.	CO2	L3
27	Prove the laws of De-Morgans both SOP and POS.	CO1	L2
28	Find all the Prime Implicants of the function $f(a,b,c,d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	CO2	L3
29	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a,b,c,d) = \sum m(4,5,7,12,14,15)$	CO2	L3
30	Find a minimal sum for the following incomplete Boolean function using decimal notation Quine Mc-cluskey method. $f(a,b,c,d) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	CO2	L3
31	Write the map entered variable K – Map for the Boolean function $f(w,x,y,z) = \sum m(2,9,10,11,13,14,15)$	CO2	L3
32	Simplify using variable entered mapping (VEM) technique and implement using basic gates. $f(a,b,c,d) = A'B'C'D' + A'B'C'D + AB C'D' + A'BC'D' + A'B'C'D' + A'B'C'D' + A'B'C'D'$	CO2	L3
e	**Experiences**	–	–

Module – 2

Title:	Combinational Logic Circuits	Appr Time:	10 Hrs
a	*Course Outcomes*	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Analyze & Design of Boolean Expressions using Decoders & Multiplexers.	CO3	L4
2	Analyze & Design of Adders & Subs tractors using K-map	CO4	L4
b	**Course schedule**	–	–
Class No	**Module Content Covered**	**CO**	**Level**
1	General approach	CO3	L2
2	Decoders–BCD decoders	CO3	L4
3	Encoders	CO3	L2
4	Digital multiplexers–using multiplexers as Boolean function generators.	CO3	L4
5	Adders and Subtractors–Cascading full adders	CO4	L3
6	Look ahead carry	CO4	L3
7	Binary comparators.	CO4	L4

8	Design methods of building blocks of combinational logics.	CO4	L4
c	**Application Areas**	**CO**	**Level**
1	To effective data exchange In communication system	CO3	L4
2	In forming ALU for desinging CPU to GPU	CO4	L4
d	**Review Questions**	–	–
1	Design a combinational logic circuit, which converts BCD code to Excess-3 code and draw the circuit diagram.	CO3	L4
2	Design a combinational logic circuit that will multiply two 2-bit binary values	CO3	L4
3	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic diagram	CO3	L4
4	Design a combinational logic circuit to find 9's complement of a BCD number	CO3	L4
5	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	CO3	L4
6	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	CO3	L4
7	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	CO3	L4
8	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0 and B= B1B0 Output: A=B, A>B, A<B.	CO3	L4
9	Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	CO3	L3
10	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	CO3	L3
11	Describe the general working principle of decoder	CO3	L2
12	With the aid of block diagram, clearly distinguish between a decoder and encoder	CO3	L2
13	Implement a full subtractor using a decoder and NAND gates	CO4	L3
14	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	CO4	L4
15	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	CO3	L4
16	Design a keypad interface to a digital system using ten line BCD encoder	CO3	L4

17	Implement a full adder using a decoder	CO3	L3
18	Implement 3-bit binary to gray code conversion by using IC 74139	CO3	L3
19	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	CO3	L4
20	Write a note on encoders.	CO3	L2
21	What are the problem associated with the basic encoder explain how can these problems be overcome by priority encoder, considering 8-bit input lines.	CO3	L2
22	Implement the multiple functions: a)$f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.	CO3	L4
23	Implement the following with a suitable decoder with active low enable input and active high output: a) $f(w,x,y,z) = \sum m(3,7,9)$ b)$f(a,b,c,d) = \pi d(2,4,7)$.	CO3	L4
24	Realize the following Boolean functions using 74139. a) $f(w,x) = \sum m(0,2)$ b) $f(a,b,c) = \sum m(1,3,6,7)$.	CO3	L4
25	Configure a 16 to 1 MUX using 4 to 1 MUX.	CO3	L4
26	Design 2-bit comparator using gates	CO3	
27	Design a 4-bit BCD adder circuit using IC7483, with self correcting circuit. ie, a provision has to be made in the circuit, in case if the sum of BCD number exceeds 9.	CO4	L4
28	Design and implement a 4-bit look ahead carry adder.	CO4	L4
29	Implement a 12-bit comparator using IC7485.	CO4	L3
30	Design a comparator to check if two n-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators.	CO4	L4
31	Design a binary full adder using minimum number of gates.	CO4	L4
32	Explain the following terms a)Ripple carry propagation b)Propagation delayc)Look ahead carry d)Iterative design.	CO4	L2
33	Design a binary full subtractor using minimum number of gates.	CO4	L4
34	Explain 4-bit Parallel adder and subtractor.	CO4	L2
35	Explain Decimal adder.	CO4	L2
36	Explain Decimal adder.	CO4	L2
37	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	CO3	L4
38	Design a full adder using MUX. For a full adder S= $\sum m(1,2,4,7)$ C = $\sum m(3,5,6,7)$	CO4	L4
39	Implement the following function using 4:1 MUX $f(a,b,c) = \sum m(1,3,5,6)$	CO3	L4
e	**Experiences**	–	–

E1. CIA EXAM – 1

a. Model Question Paper – 1

Crs Code:	17cs45	Sem:	4	Marks:	30	Time:		80 minutes		
Course:	Software engineering									
-	-	Note: Answer any 2 questions, each carry equal marks.						Marks	CO	Level
1	a	Design a logical Circuit, when Two motors M2 and M1 are controlled by three sensors S3, S2 and S1. One motor M2 is to run any when all the three sensors are ON. The other motor is to run when ever sensors S2 or S1 but not both are ON and S3 is OFF. For all sensors combinations where M1 is ON, M2 is OFF, except when all the three sensors are OFF and then both motors must remain OFF.						8	CO1	L3
	b	Reduce the following functions using K-map technique and implement using Gates. (i) $f(P,Q,R,S) = \Sigma m\ (0,1,4,8,9,10)$ (ii) $f(A,B,C,D) = \Pi M\ (0,2,4,10,11,14,15)$						8	CO1	L3
	c	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$						9	CO1	L3
		OR								
2	a	Find a minimal sum for the following incomplete Boolean function using Decimal Q-M method and prime implicant table reduction $f(a,b,c,d) = \Sigma m\ (2,3,4,5,13,15) + \Sigma d\ (8,9,10,11)$						8	CO2	L3
	b	For a given incomplete Boolean function find a minimal sum & minimal product using MEV technique using A, B & C as map variables $F(A,B,C,D) = \Sigma m\ (1,5,6,7,9,11,12,13) + \Sigma d\ (0,3,4)$						9	CO2	L3
	c	Write a note on encoders.						8	CO3	L3
3	a	Design 32:1 Multiplexer using only IC74150.						8	CO3	L4
	b	Design a combinational circuit to find 9,s complement of a BCD number, realize the circuit using suitable Logic gates.						9	CO3	L4
	c	Explain 4-bit Parallel adder and subtractor.						8	CO3	L2
4	a	Realize the following Boolean function $P=f(w,x,y,z) =\Sigma(0,1,5,6,7,10,15)$ using(i) 16 to 1 MUX (ii) 8 to 1 MUX (iii) 4 to 1 MUX						5	CO3	L3
	b	With a neat logic diagram, Explain Carry look ahead adder.						5	CO4	L2
	c	What is comparator? Design 2-bit comparator and implement with suitable logic gates.						5	CO4	L4

b. Assignment –1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions						
Crs Code:	18EC34	Sem:	3	Marks:	10/ 10	Time:	90 – 120 minutes
Course:	DSD					

Note: Each student to answer 2–3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	What are the different ways of simplifying a Boolean expression	10	CO1	L4
2	1KT18EC002	What are canonical forms illustrate with an example	10	CO1	L4
3	1KT18EC003	Reduce the following function using K-Map technique and implement using Basic gates. a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).\,dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	5	CO1	L4
4	1KT18EC004	Reduce the following function using K-Map technique and implement using only the NAND gates. a. $f(A,B,C,D) = \sum(0,2,5,7,8,10,13,15) + dc(9,11)$ b. $f(A,B,C,D) = \prod(3,4,6,11,12,14).\,dc(7,15)$ c. $f(A,B,C,D) = \sum(1,3,4,6,9,11) + dc(5,7)$ d. $f(A,B,C,D) = \prod(0,1,2,5,9,11).\,dc(7,13)$	6	CO2	L3
5	1KT18EC005	Convert the Sum of products expression to its Canonical form a. $f(a,b,c) = (ac + ab + bc)$ b. $f(a,b,c) = a.(abc)$ c. $f(a,b,c) = (ab' + bc)$	5	CO2	L3
6	1KT18EC006	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	6	CO2	L3
7	1KT18EC007	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates	10	CO2	L3
8	1KT18EC008	Staircase light is controlled by two switches; one is at the top of the stair and other at the bottom of the stairs. a.Make a truth table for this system. b.Write the logic equations in the SOP form. c.Realize the circuit using basic gates. Realize the circuit using minimum number of NAND gates	8	CO2	L3
9	1KT18EC009	Design a combinational logic circuit, which converts BCD code into Excess-3 code and draw the circuit diagram.	10	CO2	L3
10	1KT18EC010	Distinguish between prime implicants and essential prime implicants. Determine the same of the function using K-map & hence the minimal sum expression. $f(w,x,y,z) = \sum m(0,1,4,5,9,11,13,15)$	8	CO2	L3
11	1KT18EC011	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not	10	CO2	L3

		both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.			
12	1KT18EC012	Simplify the following expression using Quine-McClusky technique and implement using basic gates. $f(A, B, C, D) = \sum m(1,3,4,5,6,9,11,12,13,14)$	6	CO1	L4
13	1KT18EC013	Minimize $f(a, b, c, d) = \pi M(0,6,7,8,9,13) + \pi d(5,15)$ using Quine – McClusky method.	6	CO3	L3
14	1KT18EC014	Find all the Prime Implicants of the function $f(a, b, c, d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	10	CO3	L3
15	1KT18EC015	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a, b, c, d) = \sum m(4,5,7,12,14,15)$	6	CO4	L4
16	1KT18EC016	Find a minimal sum for the following incomplete Boolean function using decimal notation Quine Mc-cluskey method. $f(a, b, c, d) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	5	CO4	L4
17	1KT18EC017	Write the map entered variable K – Map for the Boolean function $f(w, x, y, z) = \sum m(2,9,10,11,13,14,15)$	5	CO3	L3
18	1KT18EC018	Simplify using variable entered mapping (VEM) technique and implement using basic gates. $f(a, b, c, d) = A'B'C'D' + A'B'C'D + AB'C'D' + A'BC'D' + A'B'C'D' + A'B'C'D' + A'B'C'D'$	8	CO3	L3
19	1KT18EC019	Design a combinational logic circuit, which converts BCD code to Excess-3 code and draw the circuit diagram.	6	CO4	L4
20	1KT18EC020	Design a combinational logic circuit that will multiply two 2-bit binary values	8	CO4	L4
21	1KT18EC021	Design a combinational logic circuit to output the 2's complement of a 4-bit binary numbers: a) Construct the truth table. b) Simplify each output equation using K-map an write reduced equations. c) Draw the resulting logic diagram	10	CO4	L3
22	1KT18EC022	Design a combinational logic circuit to find 9's complement of a BCD number	10	CO4	L3
23	1KT18EC001	Design a combinational logic circuit to drive a common cathode seven segment display with BCD inputs	10	CO4	L3
24	1KT18EC002	Design a combinational logic circuit to output a 1 when an illegal BCD code occurs	10	CO4	L3
25	1KT18EC003	Design a combinational logic circuit to drive a common anode seven segment display with BCD inputs	10	CO4	L3
26	1KT18EC004	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0	10	CO4	L3

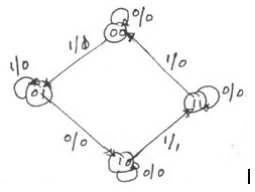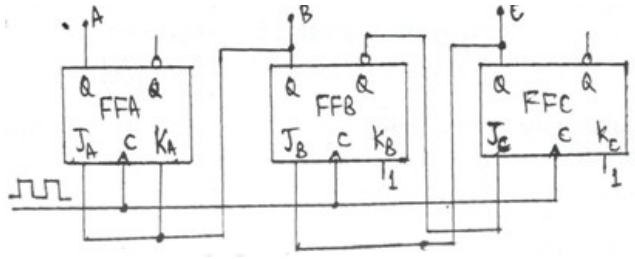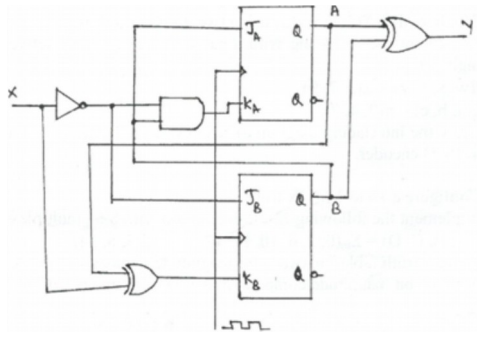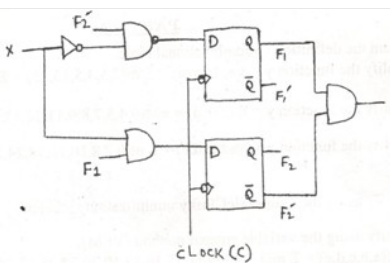| 27	1KT18EC005	and B= B1B0 Output: A=B, A>B, A<B. Develop the logic diagram of a 2 to 4 decoder with the following specifications: a)Active low enable input. b) Active high encoded outputs. Draw the IEEE symbol.	10	CO4	L3
28	1KT18EC006	Write the condensed truth table for 0,4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs	10	CO4	L3
29	1KT18EC007	Describe the general working principle of decoder	10	CO4	L3
30	1KT18EC008	With the aid of block diagram, clearly distinguish between a decoder and encoder	10	CO4	L3
31	1KT18EC009	Implement a full subtractor using a decoder and NAND gates	10	CO4	L3
32	1KT18EC010	Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit	10	CO4	L3
33	1KT18EC011	Designa 4 to 16 decoder using two 3 to 8 decoder (74LS138).	10	CO4	L3
34	1KT18EC012	Design a keypad interface to a digital system using ten line BCD encoder	10	CO4	L3
35	1KT18EC013	Implement a full adder using a decoder	10	CO4	L3
36	1KT18EC014	Implement 3–bit binary to gray code conversion by using IC 74139	10	CO4	L3
37	1KT18EC015	Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01	10	CO4	L3
38	1KT18EC016	Write a note on encoders.	10	CO4	L3
39	1KT18EC017	What are the problem associated with the basic encoder explain how can these problems be overcome by priority encoder, considering 8–bit input lines.	10	CO4	L3
40	1KT18EC018	Realize the following Boolean functions using 74139. a) $f(w,x) = \sum m(0,2)$ b) $f(a,b,c) = \sum m(1,3,6,7)$.	10	CO4	L3
41	1KT18EC019	Configure a 16 to 1 MUX using 4 to 1 MUX.	10	CO4	L3
42	1KT18EC020	Design 2–bit comparator using gates	10	CO4	L3
43	1KT18EC021	Design a 4–bit BCD adder circuit using IC7483, with self correcting circuit. ie, a provision has to be made in the circuit, in case if the sum of BCD number exceeds 9.	10	CO4	L3
44	1KT18EC022	Design and implement a 4–bit look ahead carry adder.	10	CO4	L3

D2. TEACHING PLAN – 2

Module – 3
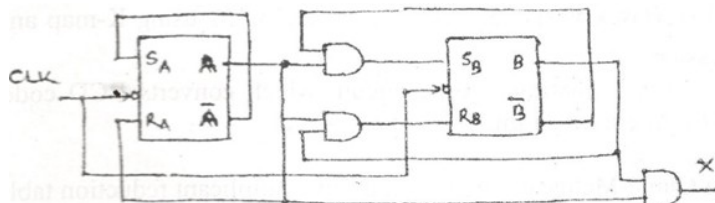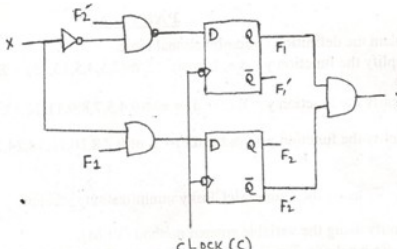
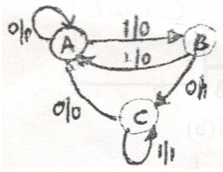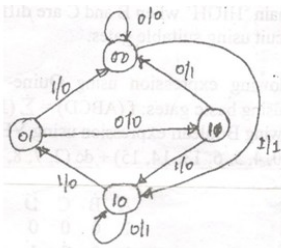| Title:	System Testing and Evaluation	Appr Time:	10 Hrs
a	*Course Outcomes*	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Understand the logics of Flip flops & Latches using Logic diagrams & verifying with truth table.	CO5	L3
2	Analyze & Design of counters using clocked D,T or SR flip flops.	CO6	L4
b	*Course Schedule*		
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Bistable element	CO5	L2
2	Latches, SR latch, application of SR latch	CO5	L2
3	A Switch debouncer	CO5	L2
4	The gated SR latch	CO5	L2
5	The gated D Latch	CO5	L2
6	The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops	CO5	L2
7	The master-slave JK Flip-Flop	CO5	L2
8	Characteristic equations	CO6	L3
9	Registers	CO6	L2
10	Counters-Binary Ripple Counter	CO6	L2
11	Synchronous Binary counters	CO6	L2
12	Counters based on Shift Registers	CO6	L2
13	Design of a Synchronous counters	CO6	L4
14	Design of a Synchronous Mod-6 counters using clocked JK Flip-Flops	CO6	L4
15	Design of a Synchronous Mod-6 counter using clocked D, T, or SR Flip Flops	CO6	L4
c	**Application Areas**	**CO**	**Level**
1	In formation of Registers	CO5	L2
2	To Set an AC timer, Flashing indicator lights of your vehicle, etc	CO6	L4
d	**Review Questions**	–	–
1	Explain with timing diagram the working of SR Latch as a switch debouncer	CO5	L2
2	Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.	CO5	L2
3	What is the significance of edge triggering? Explain the working of edge triggered D – flip flop and T – Flip flop with their functional table.	CO5	L2
4	What is a Flip Flop? Discuss the working principle of SR Flip Flop with its	CO5	L2

	truth table. Also highlight the role of SR Flip Flop in switch debouncer circuit		
5	With neat schematic diagram of master slave JK–FF, discuss its operation. Mention the advantages of JK–FF over master–slave SR–flip–flop .	CO5	L2
6	Clearly distinguish between a.Synchronous and asynchronous circuits. b.Combinational and sequential circuits	CO5	L2
7	Explain the operation of clocked SR flip–flop	CO5	L2
8	What is race around condition? Discuss in detail.	CO5	L2
9	Explain the operation of SR latch. Explain one of its applications	CO5	L2
10	What is the difference between a flip flop and a latch? What is gated SR Latch?	CO5	L2
11	Explain the operation of gated SR Latch, With a logic diagram, Truth table and logic symbol.	CO5	L2
12	Explain the operation of positive–edge–triggered JK flip–flop and T flip–flop, with the help of logic diagram, function table and logic symbol.	CO5	L2
e	Experiences	–	–
1			
2			

Module – 4

Title:	Project planning and Quality management	Appr Time:	10 Hrs
a	*Course Outcomes*	–	Blooms
–	The student should be able to:	–	Level
1	Understand the Mealy & Moore models using their Block diagrams.	CO7	L2
2	Analyze & Design of Sequential circuits using State & state transition technique.	CO8	L4
b	*Course Schedule*		
Class No	Module Content Covered	CO	Level
1	Introduction	CO7	L2
2	Mealy and Moore models	CO7	L2
3	State machine notation	CO8	L2
4	synchronous sequential circuit analysis and design.	CO8	L4
5	Construction of state Diagrams	CO8	L4
6	Counters Design.	CO8	L4
c	Application Areas	CO	Level
1	To designing the sequential circuits.	CO7	L2

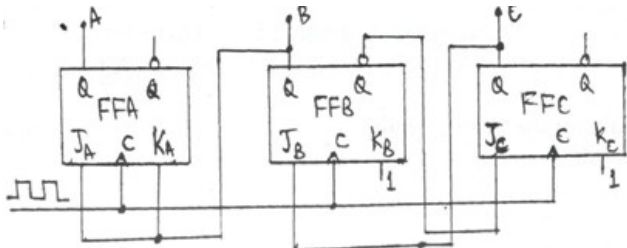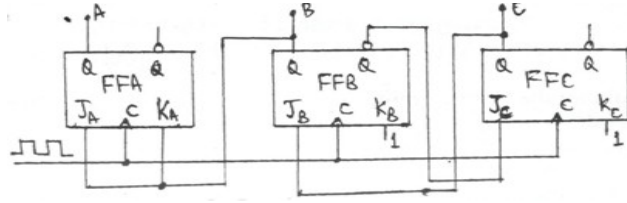|			
2	To design Elevator, vending machine, etc.	CO8	L4
d	**Review Questions**	–	–
1	Explain Mealy ad Moore sequential circuit models.	CO7	L2
2	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	CO8	
3	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop.	CO8	L4
4	Compare mealy and moore models.	CO7	L2
5	Analyse the synchronous sequential circuit shown in the figure below.	CO8	L4
6	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in figure.	CO8	L4
7	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations	CO8	L4

	c)Construct a transition table and d)Draw the state diagram.		
8	Construct the state table for the following state diagram	CO8	L4
9	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below.	CO8	L4
10	Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in the figure.	CO8	L4

11	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	CO8	L4
12	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	CO8	L4
e	**Experiences**		–	–
1			
2			

E2. CIA EXAM – 2
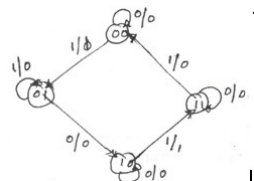
a. Model Question Paper – 2
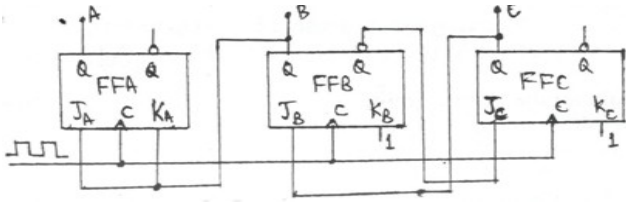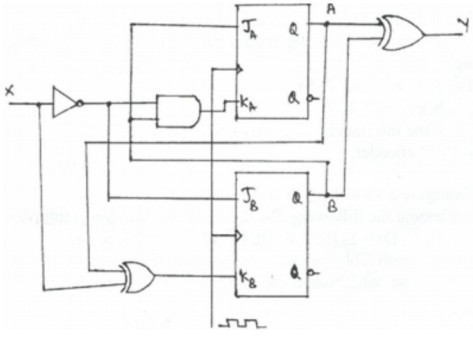
Crs Code:	18EC34	Sem:	3	Marks:	40	Time:	90 minutes
Course:	Digital System Design						

-	-	Note: Answer any 2 questions, each carry equal marks.	Marks	CO	Level
1	a	Explain the working of master slave JK flip flop with the functional table and timing diagram. Show how race around condition of master slave SR flip flop is overcome.	8	CO5	L2
	b	With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR-flip-flop .	8	CO5	L2
	c	Clearly distinguish between Synchronous and asynchronous circuits. combinational and sequential circuits.	9	CO5	L2
2	a	Explain the working of pulse triggered JK flip-flop with typical JK flip-flop waveforms.	8	CO5	L2
	b	Explain Mealy ad Moore sequential circuit models.	8	CO7	L2

	c	Analyse the synchronous sequential circuit shown in the figure below.	9	CO8	L4
3	a	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
	b	Explain Mealy ad Moore sequential circuit models.	8	CO7	L2
	c	Design a synchronous MOD–5 counter using clocked JK FF.	9	CO6	L4
4	a	Design a synchronous counter to count from 0000 to 1001 using JK flip-flops	8	CO6	L4
	b	Draw the circuit of a 3–bit asynchronous down counter using negative edge triggered JK flip-flops and draw the timing waveforms.	8	CO6	L2
	c	Design and implement a synchronous counter to count the sequence 0–3–2–5–1–0 using negative edge triggered JK flip-flops.	9	CO6	L4

b. Assignment – 2
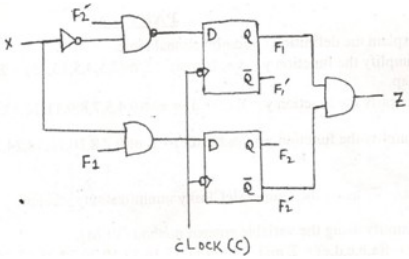
Note: A distinct assignment to be assigned to each student.

Model Assignment Questions					
Crs Code: 18EC34	Sem:	3	Marks: 10/ 10	Time:	90 – 120 minutes
Course: Digital System Design					

Note: Each student to answer 2–3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	Explain Mealy ad Moore sequential circuit models.	10	CO7	L2
2	1KT18EC002	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	10	CO8	
3	1KT18EC003	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop.	10	CO8	L4

4	1KT18EC004	Compare mealy and moore models.	10	CO7	L2
5	1KT18EC005	Analyse the synchronous sequential circuit shown in the figure below. 	10	CO8	L4
6	1KT18EC006	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in figure. 	10	CO8	L4
7	1KT18EC007	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram.	10	CO8	L4

8	1KT18EC008	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	10	CO8	L4
9	1KT18EC009	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below.	10	CO8	L4
10	1KT18EC010	Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in the figure.	10	CO8	L4
11	1KT18EC011	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	10	CO8	L4
12	1KT18EC012	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential	10	CO8	L4

		circuit with T flip-flop.			
13	1KT18EC013	Explain Mealy ad Moore sequential circuit models.	10	CO7	L2
14	1KT18EC014	Design a synchronous counter using JK flip-flops to convert the sequence 0,1,2,4,5,6,0,1,2. Use static diagram and state table	10	CO8	
15	1KT18EC015	Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop.	10	CO8	L4
16	1KT18EC016	Compare mealy and moore models.	10	CO7	L2
17	1KT18EC017	Analyse the synchronous sequential circuit shown in the figure below.	10	CO8	L4
18	1KT18EC018	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in figure.	10	CO8	L4

19	1KT18EC019	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram. 	10	CO8	L4
20	1KT18EC020	Construct the state table for the following state diagram 	10	CO8	L4
21	1KT18EC021	Give the output function, excitation table and state transition diagram by analyzing the sequential circuit shown in the figure below.	10	CO8	L4

| 22 | 1KT18EC022 | A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop. | 10 | CO8 | L4 |

D3. TEACHING PLAN – 3

Module – 5

Title:	Applications of digital circuits	Appr Time:	8Hrs
a	*Course Outcomes*	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Understand the structure of HDL, operators using block diagram & compare between VHDL & Verilog.	CO9	L2
2	Understand the structure of Data flow description using block diagram & flowchart.	CO10	L2
b	*Course Schedule*		
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction	CO9	L2
2	A brief history of HDL	CO9	L2
3	Structure of HDL Module	CO9	L2
4	Operators	CO9	L2
5	Data types	CO9	L2
6	Types of Descriptions (only VHDL)	CO9	L2
7	Simulation and synthesis	CO9	L2
8	Brief comparison of VHDL and Verilog	CO9	L2
9	Data-Flow Highlights of Data flow descriptions	CO10	L2
10	Structure of data-flow description	CO10	L2

			CO	Level
c	**Application Areas**		**CO**	**Level**
1	Used for RTL or logic level description of any digital VLSI circuits.		CO9	L2
2	Digital circuits are part of real time applications like ALU, digital clocks .		CO10	L2
d	**Review Questions**		–	–
1	Given A = 1000 and B = 0011, perform the following operations: i) A XNOR B ii) Shift B two position left logical iii) Reduction NAND iv) Verilog concatenation {A,B} v) Verilog modules A%B.		CO9	L3
2	Design a binary Multiplier using CPLDv logic		CO9	L3
3	Design Serial adder using PLD Logic		CO9	L3
4	Derive the characteristics equations of SR and JK Flip Flops.		CO9	L3
5	With a neat circuit diagram, explain the working of a universal shift register.		CO10	L3
6	Design a synchronous MOD–6 counter using clocked JK FF.		CO10	L3
7	With neat diagram and counting sequence explain synchronous MOD–10 counter.		CO10	L3
8	With neat diagram and counting sequence explain 4–bit binary ripple Counter.		CO10	L3
e			–	–
1				
2				

E3. CIA EXAM – 3

a. Model Question Paper – 3

Crs Code:	18EC34	Sem:		3	Marks:		40	Time:		80 minutes	
Course:	Software engineering										

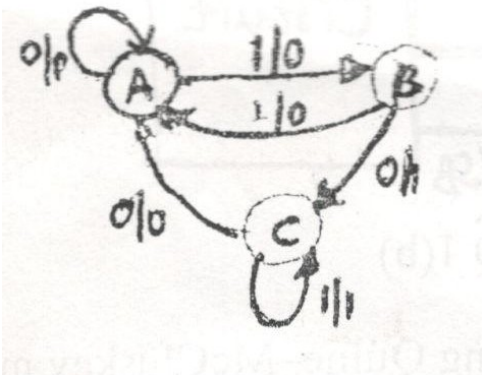| -	-	Note: Answer any 2 questions, each carry equal marks.	Marks	CO	Level
1	a	Write any two differences between mealy and moore model.	8	CO8	L2
	b	A sequential circuit has two flip-flops A and B, two inputs x and y, and an output Z. The flip-flop function and the circuit output functions are as follows: $J_A = xB + \overline{y}B$; $K_A = x\overline{y}B$; $J_B = x\overline{A}$; $K_A = x\overline{y} + A$; $Z = xyA + \overline{x}\,\overline{y}B$ Write the excitation table and transition table for the same.	9	CO8	L4
	c	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	8	CO8	L4

2	a	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with T flip-flop.	8	CO9	L3
	b	Construct the state table for the following state diagram.	9	CO9	L4
	c	What is race around condition? Discuss in detail.	9	CO9	L4
3	a	What are the steps to be followed for the design of sequential circuits?	8	CO10	L2
	b	Draw the state diagram of a Mealy machine to detect as input sequence 10110 with overlap. An output 1 is to be generated on when the sequence is detected.	8	CO10	L2
	c	Design a cyclic modulo-8 synchronous counter using T flip-flop that will count the number of occurrences of an input; that is, the number of times it is 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary.	9	CO10	L2
4	a	Design a binary Multiplier using CPLDv logic	8	CO10	L3
	b	Design Serial adder using PLD Logic	8	CO10	L3
	c	Derive the characteristics equations of SR and JK Flip Flops.	9	CO10	L3

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions								
Crs Code:	18EC34	Sem:		3	Marks:	10/ 10	Time:	90 – 120 minutes
Course:	Digital System Design							

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT18EC001	Derive the characteristics equations of SR and JK Flip Flops.	10	CO9	L3
2	1KT18EC002	With a neat circuit diagram, explain the working of a universal shift register.	10	CO9	L3

3	1KT18EC003	Design a synchronous MOD–6 counter using clocked JK FF.	10	CO9	L3
4	1KT18EC004	With neat diagram and counting sequence explain synchronous MOD–10 counter.	10	CO9	L3
5	1KT18EC005	With neat diagram and counting sequence explain 4–bit binary ripple Counter.	10	CO9	L3
6	1KT18EC006	Write the differences between Synchronous and Asynchronous counters.	10	CO9	L3
7	1KT18EC007	Design a synchronous MOD–5 counter using clocked JK FF.	10	CO9	L3
8	1KT18EC008	Derive the characteristics equations of D and T Flip Flops.	10	CO9	L3
9	1KT18EC009	Explain the working principle of mod–8 binary ripple counter, configured using positive edge triggered T–FF. also draw the timing diagram.	10	CO9	L3
10	1KT18EC010	Design Mod–6 synchronous counter using JK flip–flop	10	CO9	L3
11	1KT18EC011	Design a synchronous counter to count from 0000 to 1001 using JK flip–flops	10	CO9	L3
12	1KT18EC012	Draw the circuit of a 3–bit asynchronous down counter using negative edge triggered JK flip–flops and draw the timing waveforms.	10	CO9	L3
13	1KT18EC013	Design and implement a synchronous counter to count the sequence 0–3–2–5–1–0 using negative edge triggered JK flip–flops.	10	CO9	L3
14	1KT18EC014	Derive the characteristics equations of SR and JK Flip Flops.	10	CO9	L3
15	1KT18EC015	With a neat circuit diagram, explain the working of a universal shift register.	10	CO9	L3
16	1KT18EC016	Design a synchronous MOD–6 counter using clocked JK FF.	10	CO9	L3
17	1KT18EC017	With neat diagram and counting sequence explain synchronous MOD–10 counter.	10	CO9	L3
18	1KT18EC018	With neat diagram and counting sequence explain 4–bit binary ripple Counter.	10	CO10	L3
19	1KT18EC019	Write the differences between Synchronous and Asynchronous counters.	10	CO10	L3
20	1KT18EC020	Design a synchronous MOD–5 counter using clocked JK FF.	10	CO10	L3
21	1KT18EC021	Derive the characteristics equations of D and T Flip Flops.	10	CO10	L3
22	1KT18EC022	Explain the working principle of mod–8 binary ripple counter, configured using positive edge triggered T–FF. also draw the timing diagram.	10	CO10	L3
23	1KT18EC020	Design Mod–6 synchronous counter using JK flip–flop	10	CO10	L3
24	1KT18EC021	Design a synchronous counter to count from 0000 to 1001 using JK flip–flops	10	CO10	L3
25	1KT18EC022	Draw the circuit of a 3–bit asynchronous down counter using negative edge triggered JK flip–flops and draw the timing waveforms.	10	CO10	L3

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F. EXAM PREPARATION

1. University Model Question Paper

Course:		Digital System Design					Month / Year	Dec /2018		
Crs Code:		18EC34	Sem:	3	Marks:	100	Time:	180 minutes		
–	**Note**	Answer any FIVE full questions. All questions carry equal marks.						**Marks**	**CO**	**Level**
1	a	Explain combinational logic Circuit with the help of block diagram						5	C01	L2
	b	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$						8	C01	L2
	c	Design a logic circuit that controls the passage of a signal 'A' according to the following requirement. a.Output 'X' will equal 'A' when control inputs B and C are the same. b.'X' will remain 'HIGH' when B and C are different. Implement the circuit using suitable gates						7	C02	L3
		OR								
	a	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.						7	C01	L3
–	b	Express the following SOP expressions into minterm list form and hence write maxterm list. a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$						6	C01	L3
	c	For the following Boolean function use the Quine Mc-Cluskey method to obtain all the prime implicants and apply Petrick's method to find the irredundant disjunctive normal expressions and identify the minimal sums. $f(a,b,c,d) = \sum m(4,5,7,12,14,15)$						7	CO2	L3
2	a	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.						7	C02	L3
	b	Implement the multiple functions: a)$f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.						6	CO3	L4
2	a	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$						7	CO4	L4

	b	Design and implement a 4–bit look ahead carry adder.	8	CO4	L4
	c	Configure a 16 to 1 MUX using 4 to 1 MUX.	5	CO4	L3
3	a	Derive the characteristics equations of D and T Flip Flops.	6	CO6	L3
–	b	Explain the working of SR flip flop with diagrams	5	CO5	L2
	c	Explain Gated SR and Gated D flip–flop with waveforms	8	CO8	L4
		OR			
3	a	Explain the following: a.Switch debouncing and its elimination. b.Race around problem and its elimination	8	CO5	L2
	b	Derive the characteristics equations of SR and JK Flip Flops.	6	CO6	L3
	c	Derive the characteristics equations of D and T Flip Flops.	6	CO6	L3
4	a	Explain Mealy and Moore Model with block diagram	10	CO5	L2
	b	Design a synchronous MOD 5 counter with necessary diagrams	10	CO8	L4
		OR			
4	a	Compare Gate logic ,PLD and IC logic with atleast 5 features.	5	CO9	L2
	b	Write a switch level description for the inverter circuit with nmos and pmos.	7	CO9	L2
	c	Given A = 1000 and B = 0011, perform the following operations: i) A XNOR B ii) Shift B two position left logical iii) Reduction NAND iv) Verilog concatenation {A,B} v) Verilog modules A%B.	8	CO9	L3
5	a	Explicate the structure of verilog module.	6	C09	L2
	b	Describe scalar data type used in VHDL.	7	C10	L2
	c	Write behavioral description of the full adder circuit using VHDL and verilog.	7	CO10	L2
		OR			
5	a	With a neat circuit diagram, explain the working of a universal shift register.	7	CO10	L2
	b	Design a synchronous MOD–6 counter using clocked JK FF.	8	CO10	L4
	c	With neat diagram and counting sequence explain synchronous MOD–10 counter.	5	CO10	L2

2. SEE Important Questions

Course:	DSD						Month / Year	
Crs Code:	18EC34	Sem:		3	Marks:	100	Time:	180 minutes
	Note	Answer any FIVE full questions. All questions carry equal marks.					–	–

Mod ule	Qno.	Important Question	Mark s	CO	Year
1	1	Explain combinational logic Circuit with the help of block diagram	5	C01	L2
	2	Define the following terms along with appropriate examples for better explanation a.Literal b.Minterm c.Maxterm d.Canonical SOP e.Canonical POS f.Normal SOP a. $f(X,Y,Z) = \sum(0,2,4,6) + dc(7)$ b. $f(X,Y,Z) = \prod(0,3,5,6).dc(7)$ c. $f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + dc(2,11)$ d. $f(A,B,C,D) = \prod M(0,2,4,10,11,14,15)$	8	C01	L2
	3	Express the following SOP expressions into minterm list form and hence write maxterm list a. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$ b. $f(a,b,c,d) = (a'b'c + ab'd + abcd + a'b'cd + abc'd)$	6	C01	L3
	4	Find all the Prime Implicants of the function $f(a,b,c,d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ using Quine Mc-Cluskey method.	8	C02	L2
	5	Two motors M2 and M1 are controlled by three sensors S3, S2, S1. One motor M2 is to run any time all three sensors are on. The other motor is to run whenever sensors S2 or S1 but not both are on and S3 is off. For all sensor combinations where M1 is on, M2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation.	7	C02	L3
2	1	Design a Combinational Circuit that accepts two unsigned 2-bit binary no. and provides 3 outputs. Inputs: A=A1A0 and B= B1B0 Output: A=B, A>B, A<B.	5	CO3	L4
	2	Implement the multiple functions: a)$f(a,b,c,d) = \sum m(0,4,8,10,14,15)$. b) $f(a,b,c,d) = \sum m(3,7,9,13)$. Using two 3 to 8 decoders.	5	CO3	L4
	3	Implement the following Boolean function with 8:1 multiplexer $f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + \sum d(3,8,14)$	5	CO4	L4
	4	Design and implement a 4-bit look ahead carry adder.	7	CO3	L4
	5	Design a comparator to check if two n-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators.	5	CO4	L4
3	1	Explain the following:	8	CO5	L2

		a.Switch debouncing and its elimination. b.Race around problem and its elimination			
	2	Explain basic bistable element	5	CO5	L2
	3	What is meant by triggering of flip-flops? Name the different triggering methods.	5	CO5	L2
	4	Derive the characteristics equations of SR and JK Flip Flops.	6	CO6	L3
	5	Derive the characteristics equations of D and T Flip Flops.	6	CO6	L3
4	1	Understand the Mealy & Moore models using their Block diagrams.	8	CO7	L2
	2	Analyze the synchronous sequential circuit shown in the figure below.	8	CO8	L4
	3	Construct the state table for the following state diagram.	10	CO7	L4
	4	A sequential circuit has one output and one input, the state diagram is as shown in the figure. Design the sequential circuit with JK flip-flop.	8	CO8	L4
	5	For the logic diagram given in figure, a)Derive the excitation and output equations. b)Write the next state equations c)Construct a transition table and d)Draw the state diagram.	8	CO8	L4

5	1	Explicate the structure of verilog module.	5	C09	L2
	2	Describe scalar data type used in VHDL.	5	C10	L2
	3	Discuss logical and arithmetic operators used in VHDL.	6	CO5	L2
	4	Elaborate any two data types used in verilog.	4	CO5	L2
	5	Write behavioral description of the full adder circuit using VHDL and verilog.	4	CO5	L2
	6	Write a switch level description in VHDL for the inverter circuit with nmos and pmos.	6	CO5	L2

G. Content to Course Outcomes

1. TLPA Parameters

Table 1: TLPA – Example Course

Modul e-#	Course Content or Syllabus (Split module content into 2 parts which have similar concepts)	Content Teachin g Hours	Blooms' Learnin g Levels for Content	Final Bloo ms' Level	Identifie d Action Verbs for Learning	Instructi on Methods for Learning	Assessmen t Methods to Measure Learning
A	B	C	D	E	F	G	H
1	Software Crisis, Need for Software Engineering. Professional Software Development, Software Engineering Ethics. Case Studies. Models: Waterfall Model , Incremental Model and Spiral Model . Process activities.	5	L4 Analyze	L4 Anal yze	– Understa nd – Explore	Lecture	Slip test
1	Requirements Engineering Processes .Requirements Elicitation and Analysis . Functional and non-functional requirements . The software Requirements Document .Requirements Specification. Requirements validation .Requirements Management .	5	L3 Apply	L3 Appl y	–Identify –	Explanat ion	Q & A
2	Context models . Interaction models Structural models . Behavioral models . Model-driven engineering.	5	L3 Apply	L3 Appl y	– Interpret –	Descript ion	Q & A

2	Introduction to RUP , Design Principles. Object-oriented design using the UML. Design patterns. Implementation issues. Open source development.	5	L4 Analyze	L4 Analyze	– Compare –	Explanation	Q & A
3	Development testing, Test-driven development , Release testing , User testing. Test Automation.	5	L3 Apply	L3 Apply	– Illustrate –	Examine	Focused on analyzing / compare
3	Evolution processes . Program evolution dynamics. Software maintenance. Legacy system management	5	L4 Analyze	L4 Analyze	– Examine –	Description	Q & A
4	Software pricing . Plan-driven development. Project scheduling: Estimation techniques .	5	L4 Analyze	L4 Analyze	–Analyze –	Explanation	Slip test
4	Software quality. Reviews and inspections. Software measurement and metrics. Software standards.	5	L2 Understand	L2 Understand	–Identify –	Description	Q & A
5	Coping with Change , The Agile Manifesto: Values and Principles.	5	L2 Understand	L2 Understand	– Understand –	Develop	Q & A
5	SCRUM and Extreme Programming. Plan-driven and agile development . Agile project management , Scaling agile methods	5	L2 Understand	L2 Understand	–Explain –	Description	Q & A

2. Concepts and Outcomes:

Table 2: Concept to Outcome – Example Course

Module-#	Learning or Outcome from study of the Content or Syllabus	Identified Concepts from Content	Final Concept	Concept Justification (What all Learning Happened from the study of Content / Syllabus. A short word for learning or outcome)	CO Components (1.Action Verb, 2.Knowledge, 3.Condition / Methodology, 4.Benchmark)	Course Outcome Student Should be able to ...
A	I	J	K	L	M	N

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1	– Software Crisis, Need for Software Engineering. Professional Software Development, Software Engineering Ethics. Case Studies. Models: Waterfall Model , Incremental Model and Spiral Model . Process activities	– Software process	Software life cycle	Software process activities	–Explore –software system, component or process –system models –realistic constraints.	Explore the various types of software system
1	– Requirements Engineering Processes .Requirements Elicitation and Analysis . Functional and non-functional requirements . The software Requirements Document .Requirements Specification. Requirements validation .Requiremen	– Requirement Analysis –	Software Requirement Specifications	Requirement Analysis	–Identify –requirements for software development, –Requirements Engineering Processes.	Identify the software development requirements

	ts Management .					
2	-Context models . Interaction models Structural models . Behavioral models . Model-driven engineering.	-Model driven engineering	System Models	Development models	-Interpret -Analysis of requirements -appropriate software design	Interpret the usage of suitable software models
2	- Introduction to RUP , Design Principles. Object-oriented design using the UML. Design patterns. Implementation issues. Open source development .	-Design Analysis –	Software Design and implementation	Design techniques	-Compare -software development -Design techniques,	Compare various design techniques for software development.
3	- Development testing, Test-driven development , Release testing , User testing. Test Automation.	-Test driven development –	Software Testing	Levels of software testing	-Illustrate -software requirements and software maintenance practices -Validating	Illustrate the principles for validating the software requirements .
3	-Evolution processes . Program evolution	– Evolution process –	Software evolution	Evolution process	-Examine -Software Maintenance -Change requirement	Examine the change requirements for software

	dynamics. Software maintenance . Legacy system management					maintenance .
4	–Software pricing . Plan–driven development . Project scheduling: Estimation techniques	–Plan driven developm ent –	Software plan	Development panning	–Analyze –software project management –quality assurance procedures	Analyze the software project management plans
4	–Software quality. Reviews and inspections. Software measuremen t and metrics. Software standards.	–Software quality –	Quality management	Quality assurance procedures	–Identify –Software development process –Quality assurance procedures	Identify the quality assurance procedures
5	–Coping with Change , The Agile Manifesto: Values and Principles.	–Agile project managem ent –	Agile project management	Agile methods for software development	–Understand –Software Development –Agile project management	Understand the importance of agile project management
5	–SCRUM and Extreme Programmin g. Plan– driven and agile development . Agile project management , Scaling agile methods	–Agile method	SCRUM	Agile methods for software development	–Explain,Software development –Agile methods	Explain the Agile method for Software Development .